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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,481	09/30/2003	Feng Jin	42P17237	7521

8791 7590 06/26/2007

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EXAMINER	
ARCOS, CAROLINE H	
ART UNIT	**PAPER NUMBER**
2109	

MAIL DATE	DELIVERY MODE
06/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/676,481	JIN ET AL.	
	Examiner	Art Unit	
	Caroline Arcos	2109	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/30/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/30/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are pending.

Specification

2. The disclosure is objected to because of the following informalities:

Processes (4) through (10) on page 8 and 9 are incorrectly mentioned as part of Fig. 2 and Fig. 3. All the drawings submitted with the application don't have Processes (4) through (10).

Appropriate correction is required.

Claim Objections

3. Claims 3-5, 13, 18, 20 and 23-25 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claims 3-4 are dependant on claim 1 instead of claim 2, Claim 5 is dependant on claim 2 instead of claim 4, Claim 13 is dependant on claim 11 instead of claim 12, Claim 18 is dependant on claim 16 instead of claim 17, claim 20 is dependant on claim 16 instead of claim 19, claims 23-24 are dependant on claim 21 instead of claim 22 and claim 25 is dependant on claim 22 instead of claim 24.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 20 are rejected under 35 U.S.C 101 because it is both system and method claim which is directed to non- statutory subject matter. Claims 20 should be a method claim or a system claim, examiner interprets claims 20 as a system claims because it is dependant of a system claim.
5. Claim 21 is rejected under 35 U.S.C 101 because the claimed invention is directed to non-statutory subject matter. Claim 21 appears to be a program of software code alone (instruction) lacking the necessary physical components (hardware) to constitute a machine under 35 U.S.C 101.
6. Claims 28 are rejected under 35 U.S.C 101 because it is both machine-readable medium and a method claim, which is directed to non- statutory subject matter. Claims 28 should be a method claim or a machine-readable medium claim; examiner interprets claims 20 as a machine-readable medium claims because it is dependant of a machine-readable medium claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,6-7, 9-11, 14-15, 21, 26-27, 29-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Morrison et al (US 4,847,755)

Per claim1:

- **A method comprising: building a queue having one or more drivers** (Column 7,lines

25-28 " although it utilizes basic block information in the performance of its tasks, provides an output stream of sequential instructions without any basic block designations."), and (Column 15, lines 52-53 "The instructions within the basic blocks of the stored execution sets are stored in queues ") where, a stream of sequential instruction is a queue with one or more drivers as claimed.

- **executing the one or more drivers in the queue using a plurality of processors** (abstract, "a plurality of processor elements operates on a statically compiled program which, based upon detected natural concurrencies in the basic blocks of the programs"), and (Column 24, lines 1-2 "These instructions are assigned respectively to processors PE0, PE1, and PE2.")

- **wherein the execution of drivers by each of the plurality of processors includes determining whether there is a driver in the queue.** (Column 24, lines 1-2 "These instructions are assigned respectively to processors PE0, PE1, and PE2.") , and (Column 24, lines 12-15 "After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished.")

- **determining whether the driver is ready for execution, and if the driver is ready for execution, executing the driver.** (Column 2, lines 9-11 "the present invention conducts processing when an activity is ready for execution.")

Per claim 6:

Claim 1 is incorporated and further Morrison et al. Discloses:

- wherein the plurality of processors includes one or more logical processors. (Column 1, lines 14-15 "having a plurality of processor elements for processing the detected natural concurrencies."), and (Column 12, lines 64-65 "assign the instructions to the individual logical parallel processors.") where the plurality of processors includes one or more individual logical processors as claimed.

Per claim 7:

Claim 1 is incorporated and further Morrison et al. Discloses:

- wherein the execution of drivers in the queue further comprises removing a driver from the queue if the driver is ready for execution. (Column 2, lines 9-11 "the present invention conducts processing when an activity is ready for execution."), and (Column 5, lines 12- 14 "a new instruction enters the pipeline and a completed instruction exists the pipeline") where the pipeline is a queue and the instruction or activity is the driver removed from the queue when ready for execution as claimed.

Per claim 9:

Claim 1 is incorporated and further Morrison et al. Discloses:

- the plurality of drivers are executed in order (Column 14, lines 30-35 "Under the teachings of the present invention, basic blocks generally follow one another in the instruction stream. There may be no need for reordering of the basic blocks even though individual instructions within a basic block, as discussed above, are reordered and assigned extended intelligence information."), and (Column 48, lines 17-23 means (650) connecting said plurality of processor elements to said plurality of logical resource drivers for transferring said instruction with the earliest instruction firing time, first in said queues, from each of said logical resource drivers, in

a predetermined order, to individually assigned processor elements")

Per claim 10:

Claim 9 is incorporated and further Morrison et al. Discloses:

- wherein a first driver in the queue that has a dependency on a second driver in the queue is not executed until the second driver has been executed. (Column 8, lines 30-32 " instructions that are dependent on one another; that is, the relative ordering must be satisfied.")

Per claim 11:

A processor comprising:

- an execution unit (Column 30, lines 42-44 "This register may be loaded by the branch execution unit 1548 of the LRD as well as incremented by the cache control unit 1518 when an instruction fetch has been completed . ")

- a first logical processor and a second logical processor, the first logical processor and the second logical processor utilizing the execution unit (Column 24, lines 10-11 "the set of instructions are assigned to the logical processors on a first in time basis. After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished." Where logical processor is first logical processors and second logical processor utilizing the execution unit as claimed.

-the first logical processor to build a queue having one or more drivers(Column 7,lines 25-28 " although it utilizes basic block information in the performance of its tasks, provides

an output stream of sequential instructions without any basic block designations."), and (Column 15, lines 52-53 "The instructions within the basic blocks of the stored execution sets are stored in queues ") where, a stream of sequential instruction is a queue with one or more drivers as claimed.

- the first logical processor and the second logical processor to execute the One or more drivers in the queue in parallel at least in part (Column 8, lines13-16 "if two instructions are to execute in parallel, they must not require the same hardware element unless they are both reading that element "), and (Column 12, lines 64-65 "assign the instructions to the individual logical parallel processors.")

- wherein the execution of drivers comprising determining whether there is a driver in the queue (Column 24, lines 1-2 "These instructions are assigned respectively to processors PE0, PE1, and PE2."), and (Column 24, lines 12-15 "After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished.")

- determining whether the driver is ready for execution, and if the driver is ready for execution, executing the driver. (Column 2, lines 9-11 "the present invention conducts processing when an activity is ready for execution.")

Per claim 14:

Claim 11 is incorporated and further Morrison et al. Discloses:

- wherein the processor operates concurrently with one or more other processors. (Column 1, lines 10-15 "This invention generally relates to parallel processor computer systems and, more

particularly, to parallel processor computer systems having software for detecting natural concurrencies in instruction streams and having a plurality of processor elements for processing the detected natural concurrencies.")

Per claim 15:

Claim 11 is incorporated. Claim 15 is the processor claim of the method claim 7; it has the same limitation as claim 7 and is rejected under the same reason set forth in the connection of the rejection of claim 7.

Per claim 21:

-A machine-readable medium having stored thereon data representing sequences of instructions when executed by a processor, cause the processor to perform operations comprising: building a queue having one or more drivers (Column 7,lines 25-28 " although it utilizes basic block information in the performance of its tasks, provides an output stream of sequential instructions without any basic block designations."), and (Column 15, lines 52-53 "The instructions within the basic blocks of the stored execution sets are stored in queues ") where, a stream of sequential instruction is a queue with one or more drivers as claimed.

- executing the one or more drivers in the queue using a plurality of processors wherein the execution of drivers by each of the plurality of processors (abstract, "a plurality of processor elements operates on a statically compiled program which, based upon detected natural concurrencies in the basic blocks of the programs"), and (Column 24, lines 1-2 "These instructions are assigned respectively to processors PE0, PE1, and PE2.")

- determining Whether there is a driver in the queue, determining whether the driver is

ready for execution, and if the driver is ready for execution, executing the driver. (Column 24, lines 12-15 "After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished."), and (Column 2, lines 9-11 "the present invention conducts processing when an activity is ready for execution.")

Per claim 26:

Claim 21 is incorporated. Claim 26 is the machine-readable medium claim of the method claim 6; it has the same limitation as claim 6 and is rejected under the same reason set forth in the connection of the rejection of claim 6.

Per claim 27:

Claim 21 is incorporated. Claim 27 is the machine-readable medium claim of the method claim 7; it has the same limitation as claim 7 and is rejected under the same reason set forth in the connection of the rejection of claim 7.

Per claim 29:

Claim 21 is incorporated. Claim 29 is the machine-readable medium claim of the method claim 9; it has the same limitation as claim 9and is rejected under the same reason set forth in the connection of the rejection of claim 9.

Per claim 30:

Claim 29 is incorporated. Claim 30 is the machine-readable medium claim of the method claim 10; it has the same limitation as claim 10 and is rejected under the same reason set forth in the connection of the rejection of claim 10.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3, 16, 19 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (US 4,847,755) as applied to claims 2-3, 16, 19 and 22-23 above, and further in view of Collins (US 6,158,000)

Per claim 2:

Claim 1 is incorporated and further Morrison et al. Discloses:

- wherein a first processor of the plurality of processors is a bootstrap processor.

Morrison et al discloses that the executions of drivers are done by a plurality of processors. Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor, however, Collins discloses the above limitation. (" Abstract, "one of the processors is designated as a bootstrap processor") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to reduce system boot-up time since using one processor for boot-up and another processors for

application.

Per claim 3:

Claim 1 is incorporated and further Morrison et al. Discloses:

- wherein the plurality of processors includes one or more application processors.

Morrison et al discloses that the executions of drivers are done by a plurality of processors. Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor, however, Collins discloses the above limitation. (abstract, "the remaining processors are designates as application processors.") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to Fasten the execution of applications when designating one or more processors especially for applications execution only.

Per claim 16:

- A system comprising a bootstrap processor Morrison et al discloses that the executions of drivers are done by a plurality of processors. Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor, however, Collins discloses the above limitation. (" Abstract, "one of the processors is designated as a bootstrap processor") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to reduce system boot-up time since using one processor for boot-up and another processors for application.

- **one or more application processors** Morrison et al discloses that the executions of drivers are done by a plurality of processors. Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor, however, Collins discloses the above limitation. (abstract, "the remaining processors are designates as application processors.") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to Fasten the execution of applications when designating one or more processors especially for applications execution only.

- **a bus** (Column 30, lines 53-55 "The instruction cache selection portion 1510 receives the instructions of an execution set from memory over bus 1524.")

- **the bootstrap processor and the one or more application processors being coupled to the bus and a flash memory coupled to the bus** Morrison et al discloses that the executions of drivers are done by a plurality of processors and the processors are coupled to the bus and memory (Column 30, lines 53-55 "The instruction cache selection portion 1510 receives the instructions of an execution set from memory over bus 1524."), and (Column 31, lines 26-29 " The instruction(s) are then delivered to the PIQ bus interface unit 1544 of the LRD 620 where it is routed to the appropriate PIQ buffers 1560 according to the logical processor number (LPN)") where memory is flash memory. Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor and one or more application processors, however, Collins discloses the above limitation. (" Abstract, "one of the processors is designated as a bootstrap processor and the remaining processors are designates as application

processors.") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to reduce system boot-up time since using one processor for boot-up and another processors for application.

- **wherein the bootstrap processor and the one or more application processors execute a plurality of drivers in parallel at least in part.** Morrison et al discloses that the executions of drivers are done by a plurality of processors in parallel (Column 16, lines 40-42 "The three processor elements PE0, PE1, and PE2 process instructions I0, I1, and I4 concurrently") Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor and one or more application processors, however, Collins discloses the above limitation. (" Abstract, "one of the processors is designated as a bootstrap processor and the remaining processors are designates as application processors.") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to reduce system boot-up time since using one processor for boot-up and another processors for application.

- **the execution of the drivers by the bootstrap processor and each of the one or more application processors including determining whether there is a driver to be executed.** Morrison et al discloses that the executions of drivers are done by a plurality of processors and determine if there is driver to be executed (Column 24, lines 12-15 "After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been

processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished.") Morrison et al did not disclose that the first processor from the plurality of processors is bootstrap processor and one or more application processors, however, Collins discloses the above limitation. (" Abstract, "one of the processors is designated as a bootstrap processor and the remaining processors are designates as application processors.") Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Collins's because one of ordinary skill in the art would be motivated to reduce system boot-up time since using one processor for boot-up and another processors for application.

-determining whether the driver is ready for execution, and if the driver is ready for execution, executing the driver. (Column 2, lines 9-11 "the present invention conducts processing when an activity is ready for execution.")

Per claim 19:

Claim 16 is incorporated. Claim 19 is the system claim of the method claim 7; it has the same limitation as claim 7 and is rejected under the same reason set forth in the connection of the rejection of claim 7.

Per claim 22:

Claim 21 is incorporated. Claim 22 is the machine-readable medium claim of the method claim 2; it has the same limitation as claim 2 and is rejected under the same reason set forth in the connection of the rejection of claim 2.

Per claim 23:

Claim 21 is incorporated. Claim 23 is the machine-readable medium claim of the method claim 3; it has the same limitation as claim 3 and is rejected under the same reason set forth in the connection of the rejection of claim 3.

9. Claims 4, 8, 12, 24, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (US 4,847,755) as applied to Claims 4, 8, 12, 24, and 28 above, and further in view of Rothman (US 004/0088231 A1).

Per claim 4:

Claim 1 is incorporated.

- **wherein if a second processor in the plurality of processors determines that there are no drivers left in the queue, the second processor goes to an idle state.** Morrison et al discloses that the determination to check for any drivers left in the queue (Column 24, lines 1-2 "These instructions are assigned respectively to processors PE0, PE1, and PE2.") and (Column 24, lines 12-15 "After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished."). Morrison et al did not disclose the case where there are no drivers left in the queue, the second processor goes idle, however, Rothman discloses the above limitation. (Page 4, paragraph 0043, lines 10-14 "The configuration controller 102 then communicates with the firmware interface database agent 110 to determine if there are any driver restarts remaining in the restart queue that need to be restarted. "), and (Page 4, paragraph 0044, lines 5-7 "Once the configuration controller 102 and the driver manager have re-initialized all of the appropriate drivers, the configuration manager 100 stops ") where the

configuration manager is the second processor as claimed. Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Rothman's because one of ordinary skill in the art would be motivated to better for performance and save CPU cycles.

Per claim 8:

Claim 1 is incorporated.

Wherein the method is utilized in an extensible firmware interface (EFI).

Morrison et al discloses that the execution of drivers are done by a plurality of processors and the determination whether the driver is ready for execution. Morrison et al did not disclose that the method is utilized in an extensible firmware interface, however, Rothman et al discloses the above limitation, (Page 2, paragraph 0017, lines 1-4 "the interface 10 is Intel's Extensible Firmware Interface (hereafter "EFI"), which is an open extensible interface that lends itself to the creation of platform drivers. Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al into Rothman's because one of ordinary skill in the art would be motivated to enhance platform capabilities such as fault tolerance or security and helps developers avoid many frustrations inherent in trying to squeeze new code into traditional basic input/output system (BIOS).

Per claim 12:

Claim 11 is incorporated. Claim 12 is the processor claim of the method claim 4; it has the same limitation as claim 4 and is rejected under the same reason set forth in the connection of the rejection of claim 4.

Per claim 24:

Claim 21 is incorporated Claim 24 is the machine-readable medium claim of the method claim 4; it has the same limitation as claim 4 and is rejected under the same reason set forth in the connection of the rejection of claim 4.

Per claim 28:

Claim 21 is incorporated. Claim 28 is the machine-readable medium claim of the method claim 8; it has the same limitation as claim 8 and is rejected under the same reason set forth in the connection of the rejection of claim 8.

10. Claims 5, 13, 17, 18, 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (US 4,847,755) as applied to Claims 5, 13, 17, 18, 20 and 25 above, and further in view of Collins (US 6,158,000) and Rothman (US 2004/0088231 A1)

Per claim 5:

Claim 2 is incorporated.

- wherein if the first processor determines there are no drivers left in the queue, the first processor: waits until all other processors in the plurality of processors are in an idle state; and boots an operating system. . Morrison et al discloses that the determination to check for any drivers left in the queue (Column 24, lines 1-2 "These instructions are assigned respectively to processors PE0, PE1, and PE2.") and (Column 24, lines 12-15 "After making the assignment, stage 1160 is entered to determine whether or not the last basic block has been processed and if not, stage 1170 brings forth the next basic block and the process is repeated until finished."). Morrison et al did not disclose that the first processor is a bootstrap processor

which was covered by Collins (" Abstract, "one of the processors is designated as a bootstrap processor") and Morrison et al did not disclose that the processor wait till all processors are idle to boot the operating system, however, Rothman discloses the above limitation. (Page 4, paragraph 0044, lines 5-7 "Once the configuration controller 102 and the driver manager have re-initialized all of the appropriate drivers, the configuration manager 100 stops (block 284) and the user is returned to a menu, or the OS 30 continues loading until it is fully operational.") where in multi-processors environment, it is inherent that configuration controller is more than one processors. Configuration controller is the first processor and the second processor that check whether the queue is empty. Once the plurality of processors finish executing all drivers in the queue, they go idle and the OS boots up as claimed. Therefore it will be obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teaching of Morrison et al and Collins' s into Rothman's because one of ordinary skill in the art would be motivated to better for performance and save CPU cycles.

Per claim 13:

Claim 11 is incorporated. Claim 13 is the processor claim of the method claim 5; it has the same limitation as claim 5 and is rejected under the same reason set forth in the connection of the rejection of claim 5.

Per claim 17:

Claim 16 is incorporated. Claim 17 is the system claim of the method claim 4; it has the same limitation as claim 4 and is rejected under the same reason set forth in the connection of the

rejection of claim 4.

Per claim 18:

Claim 16 is incorporated. . Claim 18 is the system claim of the method claim 5; it has the same limitation as claim 5 and is rejected under the same reason set forth in the connection of the rejection of claim 5.

Per claim 20:

Claim 16 is incorporated. Claim 20 is the system claim of the method claim 8; it has the same limitation as claim 8 and is rejected under the same reason set forth in the connection of the rejection of claim 8.

Per claim 25:

Claim 22 is incorporated. Claim 25 is the machine-readable medium claim of the method claim 5; it has the same limitation as claim 5 and is rejected under the same reason set forth in the connection of the rejection of claim 5.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caroline Arcos whose telephone number is 571-270-3160. The examiner can normally be reached on 7:30 AM- 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-272-3696. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Caroline Arcos
CA
Patent Examiner

CHAMELI DAS
SUPERVISORY PATENT EXAMINER
6/22/07